

A block diagram of a memory system. On the left, a vertical stack of eight rectangular cells represents an input register, labeled 10. An arrow points from this register to a central rectangular block labeled 'MEMORY' with the number 11 above it. Another arrow points from the 'MEMORY' block to a second vertical stack of eight rectangular cells on the right, labeled 17, which represents an output register. An arrow points away from the output register to the right. A return line connects the bottom of the input register 10 to the bottom of the output register 17, completing the loop.

The diagram illustrates a memory testing system. It features a central MEMORY block (11). To the left, a BIST GEN. (20) is connected to the input of a multiplexer (21). A vertical stack of memory cells (10) is also connected to the input of multiplexer 21. The output of multiplexer 21 is connected to the MEMORY block (11). To the right, the MEMORY block (11) is connected to the input of another multiplexer (22). The output of multiplexer 22 is connected to a BIST RESP. (23). A vertical stack of memory cells (12) is also connected to the output of multiplexer 22. A BIST CONTROL block (24) is connected to the BIST GEN. (20) and the BIST RESP. (23).

FIGURE 2 - PRIOR ART

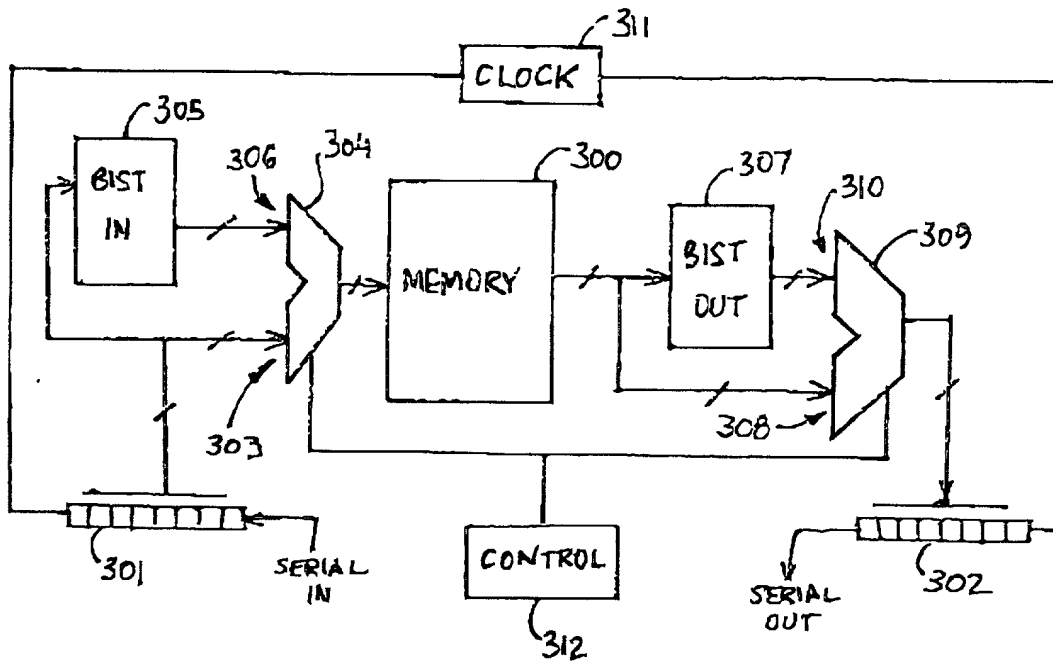


FIGURE 3

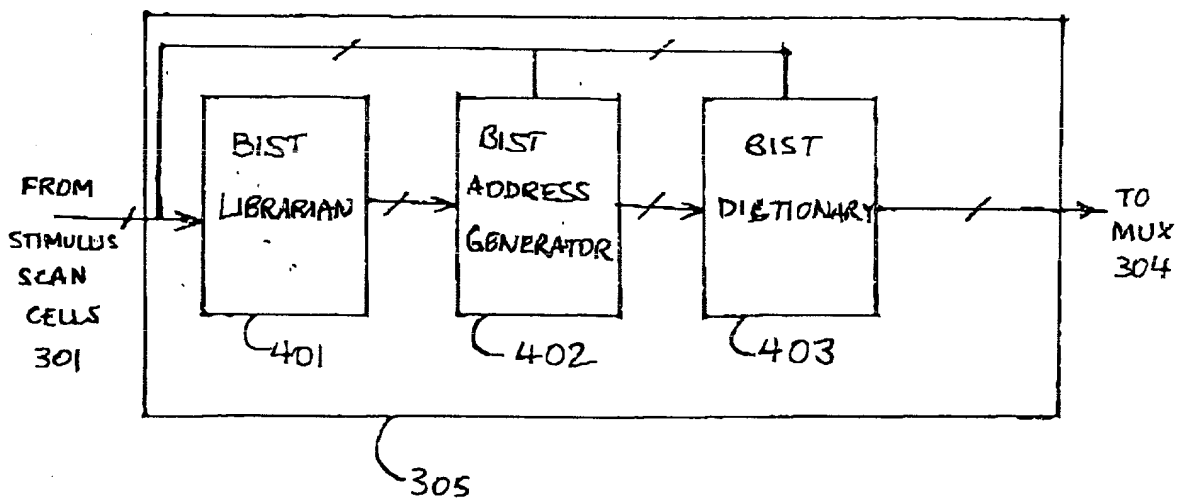


FIGURE 4